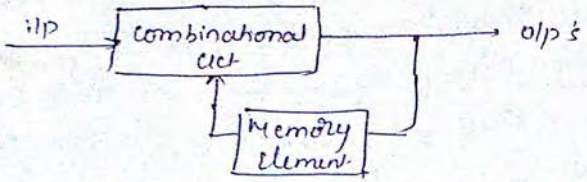
UNIT-3 (1-8).

Sequential Machine fundamentals

Basic Architectural distinction b/w combinational & sequential ckts:

Sequential ckt:

Block dia:



diff:	combinational	sequential.
1.	The o/p variables are at all times dependent on the combination of i/p variables.	The o/p variables not only depend on present i/p variable but also past history of the i/p variables.
2.	Memory unit is not required	Required to store past history of i/p variables
3.	Faster in speed bcz delay b/w i/p & o/p is due to propagation delay of gate.	Slower
4.	They are easy to design	Harder to design
5.	parallel adder is a combinational ckt.	Serial adder is seq ckt.
6.		
7.	more Expensive	Cheaper.

Classification of seq ckts — Synchronous.

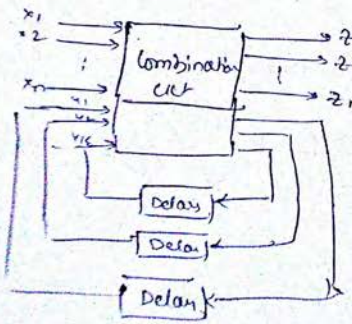
[It is classified depending on timing of their sgn.

- sgn can affect memory elements only at discrete instants of time.
- Here memory element is F-F which is capable of storing 1-bit binary information. They are clocked FF
- i/p sgn changes can effect memory element up on activation of clk sgn
- max operating speed of clk depends on time delays involved
- Easier to design, higher cost

Asynchronous.

- Change in i/p sgns can affect memory element at any instant of time.
- Memory elements are either unclocked FF (or) Time delay elements.
- change in i/p sgns can affect memory element at any instant of time.
- Because of absence of clk, These can be operated faster than synchronous ckts.
- difficult, lower cost.

Level mode & pulse mode Asynchronous sequential ckts:



n i/p variables

m o/p variables

Block dia of asynchronous seq ckt.

Present state & next state variable in asynchronous seq ckt is called secondary variables (or) & Excitation variables.

Asynchronous ckt

Fundamental mode ckts
- i/p variable changes only when the ckt is stable.
- one i/p variable can change at a given time.
- i/p's are levels and not pulses

Pulse mode ckts
- i/p variables are pulses.
- width of the pulses is long enough for the ckt to respond to the i/p.
- pulse width must not be so long that it is still present after the next state is reached.

One bit memory cell: i/p's — Q, $\bar{Q}$ — symb

* The fundamental seq ckt is latch (or) FF → bistable multivibrator device that can store 1 bit of info.

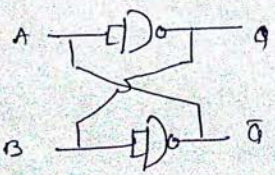
Latches & Flip Flops: There are both bistable elements.

Latches: sequential device that checks all i/p's continuously & changes it's o/p accordingly at any time independent of clocking sgn. (enable is provided)

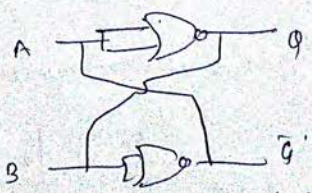
Flip Flops: used for seq devices (ie) i/p changes with o/p only when time determined by clocking sgn. (clock is provided)

- 1 bit memory cell:

using NAND!



NOR!

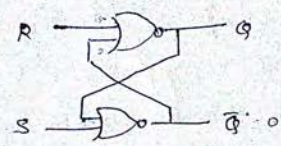


- It has two stable states — In 1 stable state Q=1 (set state)
  Q=0 (Reset state.

∴ Bit info is loaded/latched it is called latch.

S-R latch: (set-reset): can be constructed using either two NAND / NOR gate.

Using NOR: Tech called cross coupling.



NOR operation: A⊕B $\overline{A+B} \Rightarrow \bar{A}\bar{B}$

Case1: S=1 R=0 [∵ Q=1, latch is set stat]
$\bar{Q}$=0, Q=1

2: S=0 R=1 [∵ Q=0, latch is Reset stat]
$\bar{Q}$=1 Q=0

3: S=0 R=0
$\bar{Q}$=1 Assume Q=1 [Inactive stat].
$\bar{Q}$=0

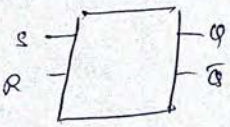
* when S=R=0, o/p stat doesn't change.

ex. Q=0, $\bar{Q}$=1 ⇒ o/p stat "

4. S=1 R=1, Q=$\bar{Q}$=0, this is called Indetermined (or) prohibited stat

Represented by asterisk (*)

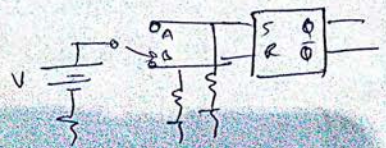
Symb.



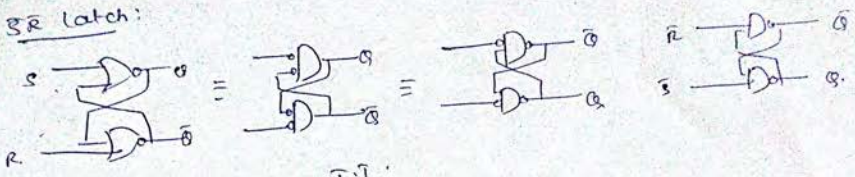
T-T.

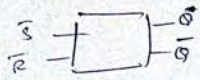
S	R	Q_n	Q_{n+1}	
0	0	0	0	Stat.
0	0	1	1	No change
0	1	0	0	
0	1	1	0	Reset
1	0	0	1	
1	0	1	1	Set
1	1	0	*	
1	1	1	*	Indetermined

Application: A switch Debouncer:



SR latch:

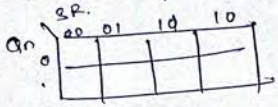




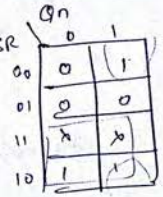
T.T.

$\bar{S}$	$\bar{R}$	Q_n	Q_{n+1}	State
0	0	0	x	Indetermined
0	0	1	x	
0	1	0	1	Set
0	1	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	0	No change
1	1	1	1	

Characteristic eqn:



(or)

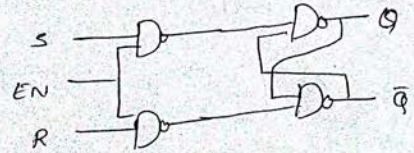


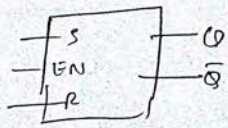
$Q_{n+1} = S + \bar{R} Q_n$.

Gated SR latch:

∴ latch is sensitive as o/p changes immediately as i/p changes.

So the modified form of latch which includes EN. is known as gated latch.



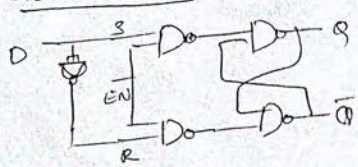


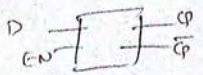
When EN=1 ⇒ behaves as SR latch

EN=0 ⇒ Retains previous state.

EN	S	R	Q_n	Q_{n+1}	state
0	×	×	0	0	No change
0	×	×	1	1	
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	set
1	1	0	1	1	
1	1	1	0	×	Indeterminate
1	1	1	1	×	

Gated D latch: (Transperant latch bcz : Q - o/p follows D i/p).





EN	D	Q_n	Q_{n+1}	
0	×	×	Q_n	No change
1	0	×	0	Reset
1	1	×	1	set

S_0	S_1	Q_0
0	0	
1	0	
1	1	

EN \ DQ_n	00	01	11	10
0	Q_n	Q_n	Q_n	Q_n
1			1	1

Char eqn: $Q_{n+1} = \bar{EN}\,Q_n + EN \cdot D$

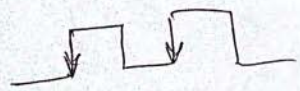
Pulsed Triggered FF:

Latches ⟶ EN i/p (sgn). so they are either +ve level triggered or -ve level triggered.

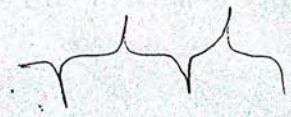
FF ⟶ pulse triggered.

level triggering

pulse.



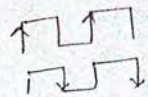
Edge triggering



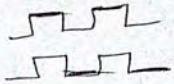
Basic FF: SR, JK, D, T

Triggering of FF

1. Edge Triggering < +ve Edge triggering / -ve Edge triggering



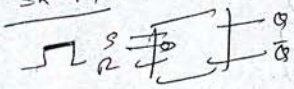
2. pulse Triggering < +ve / -ve



(or)

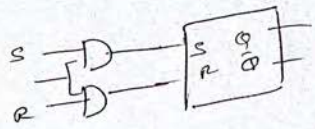
level triggering

SR FF: Set-Reset

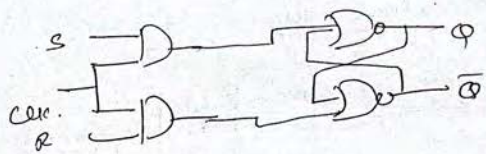


+ve level triggered

Block dia of clocked FF



with clocked NOR:



TT:

Clk	Sn	Rn	o/p Q_{n+1}	State
↑	0	0	Q_n	NC.
↑	0	1	0	R
↑	1	0	1	S
↑	1	1	X	Indetermined.

Characteristic Table:

FF i/p		present o/p	Next o/p
S	R	Q_n	Q_{n+1}
0	0	0	$Q_n = 0$
0	0	1	$Q_n = 1$
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

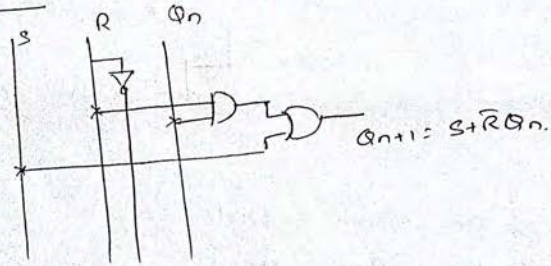
S \ R Qn	00	01	11	10
0	0	1	0	0
1	11	1	x	x

$Q_{n+1} = \bar{R} Q_n + S$.

Excitation table:

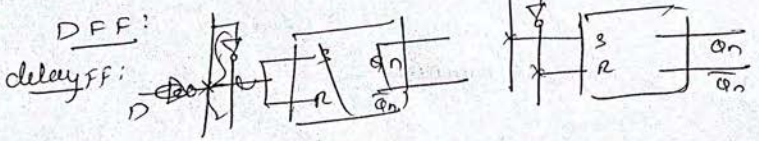
P.S Q_n	N.S Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0.

logic dia:



DFF:

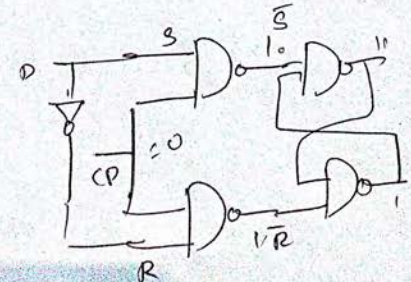
delay FF:



* The problem of indetermined condition in S=R=1 (SR FF) can be rectified by adding inverter from S to R.

logic sym

logic dia:



$C_p = 0$, P.S

$C_p = 1$, D=1

0/P = 1

C

T FF:

clk	i/p	o/p
	D	Q_{n+1}
↑	0	0
↑	1	1
0	x	N.C.

char table:

FF	P.S	N.S
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

K-map

D \ Q_n	0	1
0	0	0
1	1	1

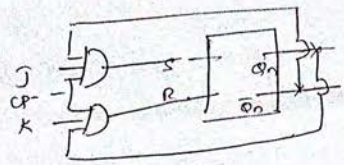
$Q_{n+1} = D$.

Excitation table:

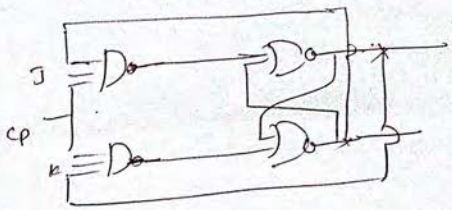
P.S	N.S	delay i/p
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

JK FF: Alternating way of eliminating indetermined condition.

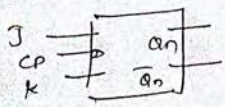
logic dia.



clocked JK FF



logic sym:



T J FF:

i/p		o/p
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Char table:

JK	P.S Q_n	N.S Q_{n+1}
0 0	0	$Q_n = 0$
0 0	1	$Q_n = 1$
0 1	0	0
0 1	1	0
1 0	0	1
1 0	1	1
1 1	0	$\bar{Q}_n = 1$
1 1	1	$\bar{Q}_n = 0$

Q_{n+1} K-map

J \ KQ_n	00	01	11	10
0	0	1	0	0
1	1	1	0	1

$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

Excitation Table.

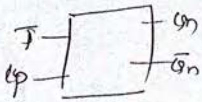
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

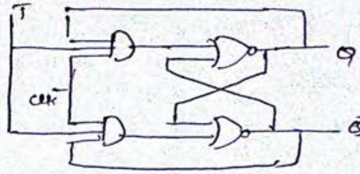
TFF: Toggle FF:

TT:

i/p T	o/p Q_{n+1}
0	

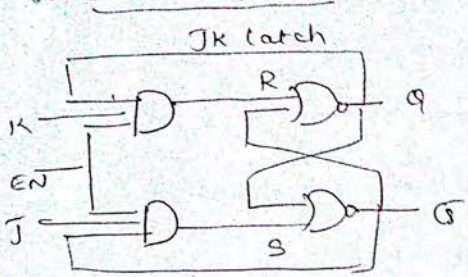
Logic symp

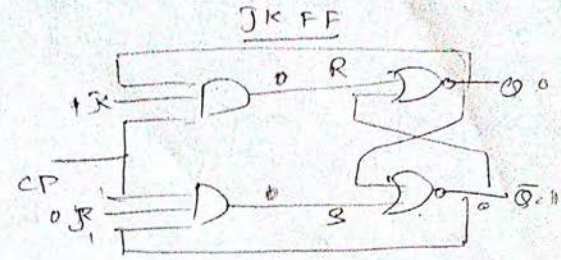




66, 71, 80, 91, 82, 86, 87, 87, 19,

* clocked JK FF:





J i/p ≡ Set i/p.
K i/p ≡ R (i/p).

∴ when SR = 11 called JK latch → to toggle (switch to complement state)

(i.e) J = K = 1, then $Q_{n+1} = \bar{Q}_n$

* when Q & $\bar{Q}$ is connected back to J & K excitation i/p, the indetermined condition that exists in SR latch is no longer indetermined.

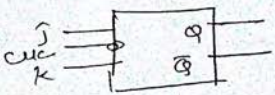
* JK latch is not practical bcz. when J = 1 = K, o/p toggles continuously. This condition is called "Race around condition" (this must be avoided.

edge triggered or pulse triggered.

* The race around condition in JK latch is nothing but propagation delay in JK FF.

* To avoid that create edge triggering or pulse triggering.

* clocked JK FF:



Q_n	J	K	Q_{n+1}	
0	0	0	0	No change
0	0	1	0	
0	1	0	1	
0	1	1	1	
1	0	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	

≡

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

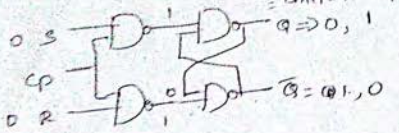
Characteristic equ.

Q_n \ JK	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

$J\bar{Q}_n + \bar{K}Q_n$

Clocked SR FF:



$Q_{n+1}=1$ $Q \Rightarrow 0, 1$ $\bar{Q}=0, 1, 0$

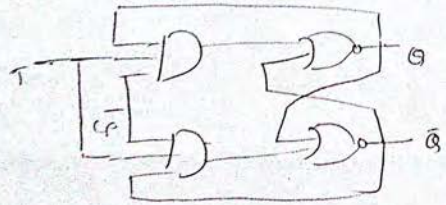
$Q=0$ $\bar{Q}=1$

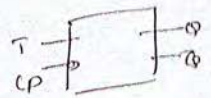
CP	S	R	Q_n	Q_{n+1}	State
↑	0	0	0	0	NC
↑	0	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	x	Indeterminate
↑	1	1	1	x	
0	x	x	0	0	NC
0	x	x	1	1	

S \ R.Q_n	00	01	11	10
0	0	1	0	0
1	1	1	x	x

$Q_{n+1} = Q_n + S\bar{R}Q_n$

T FF: Toggle:





Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

⇒

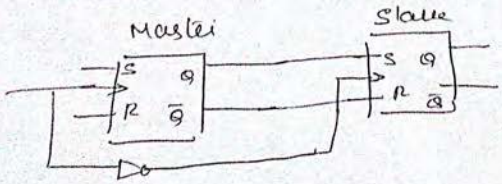
Tn	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

Q_n \ T	0	1
0	0	1
1	1	0

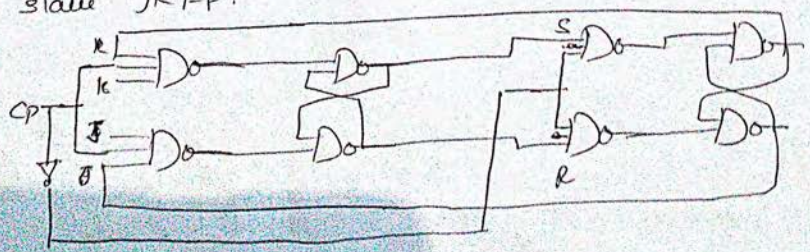
$\Rightarrow Q_{n+1} = \bar{Q}_n T + Q_n \bar{T}$

Master slave SR FF:

T is same as clocked SR FF

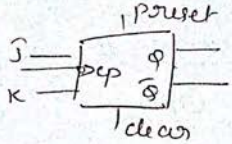


Master slave JK FF:

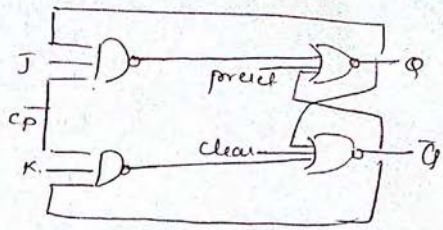


Asynchronous / Direct i/p's:

FF available in ic package sometimes provide special i/p's for preset & clear then FF is asynchronous.

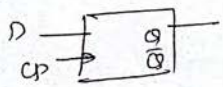


JK FF with active high preset & clear:

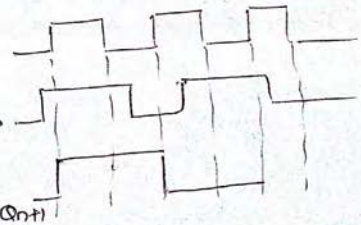


preset & clear = low for synchronous operation.

+ve Edge Triggered DFF:



cp	D	Q_{n+1}
↑	0	0
↑	1	1
0	X	Q_n. Q_{n+1}



Char eqn:

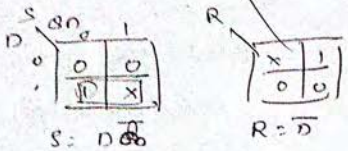
FF	Char eqn
D	$Q_{n+1} = D$
JK	$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$
T	$Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$
SR	$Q_{n+1} = S + \bar{R}Q_n$.

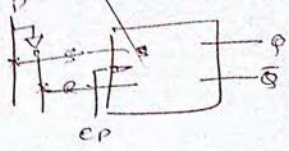
FF conversion:

SR FF to DFF:

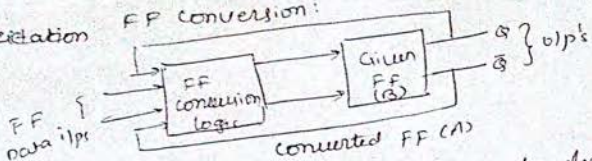
Excitation table:

i/p	present state	Next state	F·F i/p's	
D	Q_n	Q_{n+1}	S	R
0	0	0	0	x
0	1	0	0	1
1	0	1	1	0
1	1	1	x	0





Excitation FF conversion:



1. obtain present state, Next state table for desired FF(A)
2. using excitation table / application table of chosen FF(B), append nx state code (S) excitation i/p values to above present state - nxt state table.
3. using K-map, simplify.
4. Draw ckt.

SR FF to D FF:

1. PS-NS - Table of DFF

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

SR	Q_{n+1}	Q_n Q_{n+1}
0 0	Q_n	0 0
0 1	0	1 0
1 0	1	0 1
1 1	x	1 1

2.

D	Q_n	Q_{n+1}	S	R
0	0	0	0	x
0	1	0	1	0
1	0	1	0	1
1	1	1		

Excitation table :

RS FF :

Present			Next	
R S	Q_n	$\bar{Q}_{n+1}$	Q	$\bar{Q}$
0 0	0	1	$Q_n=0$	
0 0	1	0	$Q_n=1$	
0 1	0	1	1	
0 1	1	0	1	
1 0	0	1	0	
1 0	1	0	0	
1 1	0	1	x	
1 1	1	0	x	

Q_n	Q_{n+1}	S R
0	0	x 0
0	1	1 0
1	0	0 1
1	1	x 0

o/p ⇒ 0 to 0

SR = 00 ⇒ 0x

0 to 1

SR = 10

1 to 0

SR = 01 ⇒ 01

1 to 1

SR = 00 10 ⇒ x0

JK FF :

J K	Q_n	Q_{n+1}
0 0	0	
0 0	1	
0 1	0	
0 1	1	
1 0	0	
1 0	1	
1 1	0	
1 1	1	

Q_{n+1}
$Q_n = 0$
$Q_n = 1$
0
0
1
1
$\bar{Q}_n = 1$
$Q_n = 0$

Excitation table

Q_n	Q_{n+1}	J K
0	0	0 x
0	1	1 x
1	0	x 1
1	1	x 0

0 to 0 ⇒ JK = 00, 01 ⇒ 0x

0 to 1 ⇒ JK = 10, 11 ⇒ 1x

1 to 0 ⇒ JK = 01, 11 ⇒ x1

1 to 1 ⇒ JK = 00, 10 ⇒ x0

DFF:

TT

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$\therefore$ $0 \rightarrow 0$ $D = 0$

$0 \rightarrow 1$ $D = 1$

$1 \rightarrow 0$ $D = 0$

$1 \rightarrow 1$ $D = 1$

Excitation

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

TFF

T	Q_n	Q_{n+1}	
0	0	0	$Q_n = 0$
0	1	1	$Q_n = 1$
1	0	1	$\overline{Q_n} = 1$
1	1	0	$\overline{Q_n} = 0$

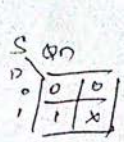
Ex: Table

Q_n	Q_{n+1}	T	
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

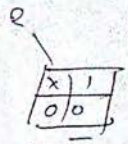
FF conversion:

SR to D.

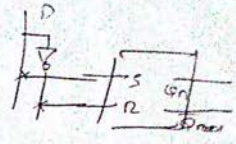
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0



$S = D$

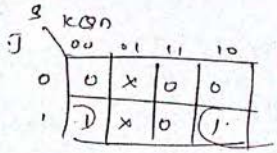


$R = \bar{D}$

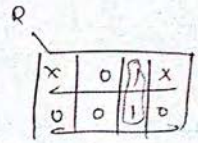


SR to JK

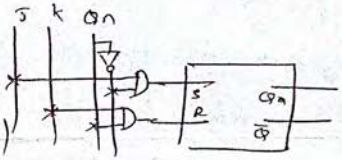
J	K	Q_n	Q_{n+1}	S	R
0	0	0	$Q_n = 0$	0	X
0	0	1	$Q_n = 1$	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	$\bar{Q}_n = 1$	1	0
1	1	1	$\bar{Q}_n = 0$	0	1



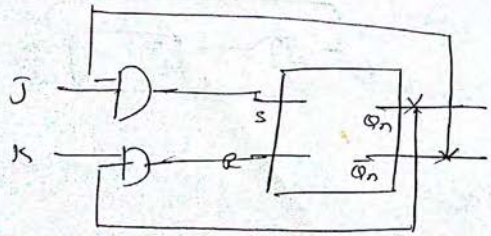
$S = J\bar{Q}_n$



$R = KQ_n$



(OR)

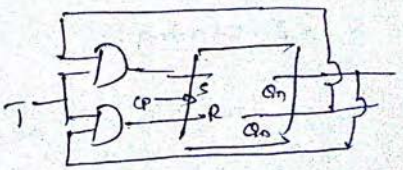


SR to T:

T	Q_n	Q_{n+1}	S	R
0	0	$Q_n = 0$	0	X
0	1	$Q_n = 1$	X	0
1	0	$\bar{Q}_n = 1$	1	0
1	1	$\bar{Q}_n = 0$	0	1

$S = T\bar{Q}_n$

$R = TQ_n$



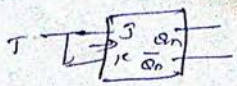
A3, B1, B3, B4,
B3, B4, A0, 90, 66
B3, B4, B0

JK to T:

T	Q_n	Q_{n+1}	J	K
0	0	0	0	x
0	1	1	x	0
1	0	1	1	x
1	1	0	x	1

$J = T$

$K = T$

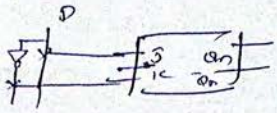


JK to D:

D	Q_n	Q_{n+1}	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

$J = D$

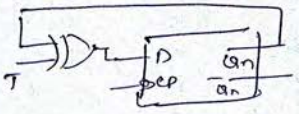
$K = \bar{D}$



D to T:

T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

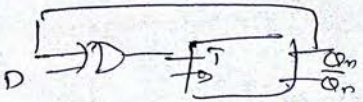
$D = T \oplus Q_n$



T to D:

D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

$T = D\bar{Q}_n + \bar{D}Q_n$



FF Timing:

Flip Flop Timing:

- Setup time
- hold time
- propagation delay.

Set up time: Min time required to maintain a constant voltage levels (data) at the excitation i/p's of the FF device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the FF. (t_{setup}).

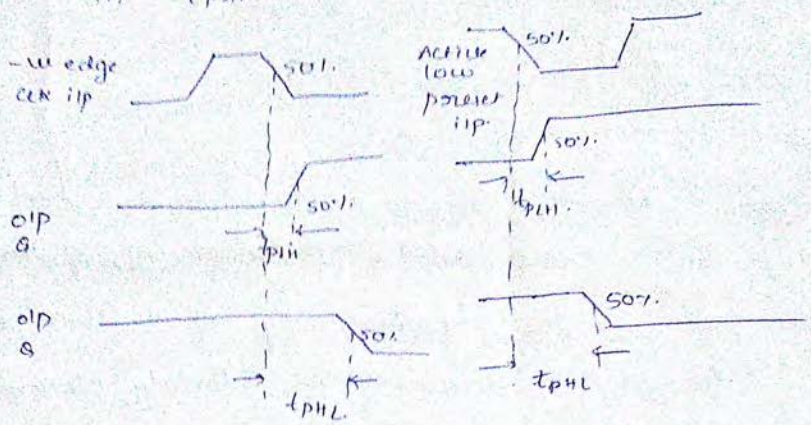
Hold time: Time for which the voltage levels (data) at the excitation i/p's must remain constant after the triggering edge of clk pulse in order for the levels to be reliably clocked into the FF. (t_{hold}).

propagation delay: Time required to change the o/p. after application of the i/p.

1) propagation delay (t_{pLH}): It is measured from triggering edge of clk pulse / preset i/p to the L-to-H transition of the o/p.

2) (t_{pHL}): Triggering edge of clk pulse or clear i/p to H to L transition of o/p.

iii) t_{PLH}:



set up & Hold time: